REMARKS/ARGUMENTS

Pending claims 1-17 and 22-25 stand rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,784,331 (Lysinger). Applicants respectfully traverse the rejection. As to claim 1, Lysinger nowhere teaches sensing a first word group from a first address of a memory while sensing a second word group from a second address of the memory. In this regard, the Office Action refers to col. 19, lns. 52-57 of Lysinger, as well as col. 20, lns. 9-13 and col. 4, lns. 15-27. None of these cited portions or anywhere else in Lysinger however, teach or suggest such simultaneous sensing of different word groups from different addresses in a memory. Instead, Lysinger merely teaches the conventional manner of sensing data of a single address at a given time. That is, as described in Lysinger, "in response to the column select signals, a sense amplifier and storage register circuit 712 senses the data from the addressed memory cells and stores that data in respective storage registers." Lysinger, col. 19, lns 19-23. Thus only sensing of a single word group from a first address is performed at a given time.

While Lysinger teaches that data is burst out of storage registers of a sense amplifier and storage register circuit at the same time that address data of another address location is decoded (Lysinger, col. 11, ln. 67 – col. 20, ln. 9), this nowhere teaches or suggests the recited sensing of two word groups from different addresses simultaneously. Accordingly, claims 1 and 22 and the claims depending therefrom are patentable over Lysinger.

For similar reasons, claim 8 is patentable as Lysinger nowhere teaches sensing a first burst length of data equal to half of a sense width of a plurality of sense amplifiers of a memory. This is so, as described above instead Lysinger teaches that all of the sense amplifiers operate in parallel to sense data of a full sense width, not a half sense width. Furthermore, Lysinger nowhere teaches sensing a second burst length of a half sense width during a latency before reading the first burst length of data. Instead, as conceded by the Office Action, Lysinger teaches that a second access occurs "while data is burst counted out of the memory device" Office Action, p. 3 (citing Lysinger, col. 20, lns. 9-13). Because this second access occurs <u>while</u> data is burst counted out of the memory device, i.e., after a latency before reading the data, claim 8 is further patentable for this reason. Thus claim 8 and the claims depending therefrom are patentable.

For at least similar reasons, claim 12 is patentable over Lysinger for the reason that Lysinger nowhere teaches that a second address of a second read operation is to be sensed at

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least partially during a latency of a first read operation. Accordingly, claim 12 and its dependent claims are patentable.

With regard to independent claim 18, which stands rejected under 35 U.S.C. §103(a) in view of Lysinger, this rejection is also improper. In this regard, for the same reasons described above, Lysinger nowhere teaches a sense array that overlappingly senses first and second word groups from first and second addresses. Instead, as described above, Lysinger merely teaches that "a sense amplifier and storage register circuit 712 senses the data from the addressed memory cells and stores that data in respective storage registers." Lysinger, col. 19, lns. 19-22.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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